

Migration from TSC87C52 to TS87C52X2

1. Introduction

This application note compares the features, SFRs, AC&DC parameters between TSC87C52 of Atmel Wireless & Microcontrollers and the new TS87C52X2. It shows the differences in the DC and AC characteristics and also the different SFR settings. It should also be noted that the new Atmel Wireless & Microcontrollers TS87C52X2 core includes the programmable clock doubler feature which is described in the application note available on our website. It shows the differences in the DC and AC characteristics and also the different SFR settings .

2. Feature Improvement

	TSC87C52	TS87C52X2
256b RAM	Yes	Yes
32 I/Os	Yes	Yes
3 16 bit-Timers	Yes	Yes
Timer 2 : Clock output mode	No	Yes
Timer 2 : Auto reload Up/Down mode	No	Yes
6 Interrupt Sources	Yes	Yes
4 priority level interrupt system	No	Yes
Wake up from Power Down by INT0 & INT1	No	Yes
UART	yes	Yes
Enhanced UART	No	Yes
Framing error detection	Yes	Yes
Multiprocessor communication	No	Yes
X2 Mode	No	Yes
Dual Data Pointer	No	Yes
Power Off Flag	No	Yes
Commercial Temperature	Yes	Yes
Industrial Temperature	Yes	Yes
Asynchronous port reset	No	Yes
Maximum Frequency @ 5V	33 MHz	40 MHz X1 mode 60 MHz eq. X2 mode
Maximum Frequency @ 3V	16 Mhz	30 MHz X1 mode 40 MHz eq. X2 mode

X1 mode is standard mode (12 clocks per instruction)

X2 mode is new mode (6 clocks per instruction)

3. SFR Mapping

Hereafter a SFR mapping comparison table between TSC87C52 and TS87C52X2.

TSC87C52

PCON Register (Sfr:87h)

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	PD	IDL

Reset Value : 000x 0000b

TS87C52X2

PCON Register (Sfr:87h)

7	6	5	4	3	2	1	0
SMOD 1	SMOD 0	-	POF	GF1	GF0	PD	IDL

Reset Value : 00x1 0000b

Comments : Power On flag , EUART

TSC87C52

Reserved Register (Sfr:8Fh)

TS87C52X2

CKCON Register (Sfr:8Fh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	X2

Reset Value : xxxx xxx0b

Comments : X2 mode

TSC87C52

SCON Register (Sfr:98h)

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Reset Value : 0000 0000b

TS87C52X2

SCON Register (Sfr:98h)

7	6	5	4	3	2	1	0
FE/ SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Reset Value : 0000 0000b

Comments : EUART : FE/SM0 Framing Error

TSC87C52

Reserved (Sfr:0A2h)

TS807C52X2

AUXR1 Register (Sfr:0A2h)

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS

Reset Value : xxxx 00x0b

Comments : Dual DPTR

TSC8752

Reserved (Sfr:0A9h)

TS87C52X2

SADDR Register (Sfr:0A9h)

7	6	5	4	3	2	1	0

Reset Value : 0000 0000b

Comments : EUART : Multiprocessor communication

TSC87C52

Reserved (Sfr:0B7h)

TS87C52X2

IPH Register (Sfr:0B7h)

7	6	5	4	3	2	1	0
-	-	-	PSH	PT1H	PX1H	PT0H	PX0H

Reset Value : xxx0 0000b

Comments : 4 level priority interrupt

TSC87C52

Reserved (Sfr:0B9h)

TS87C52X2

SADEN Register (Sfr:0B9h)

7	6	5	4	3	2	1	0

Reset Value : 0000 0000b

Comments : EUART : Multi processor communication

All other registers are identical

4. DC Parameters

$V_{CC} = 2.7V$ to $5.5V$ $\pm 10\%$; $T = -40^{\circ}$ to $+85^{\circ}C$ or $T = 0^{\circ}$ to $70^{\circ}C$

Symbol	Parameters	TSC87C52		TS87C52X2		Unit	Comments
		Min	Max	Min	Max		
VIH	Input High Voltage except XTAL1, RST	$0.2V_{CC}+1.4$		$0.2V_{CC}+0.9$		V	
IPD	Power Down Current		75		50	μA	$V_{CC} = 2.0V$ to $5.5V$

5. AC parameters

5.1. External Program Memory Characteristics

Symbol	Parameter	Cond.	TSC87C52	TS87C52X2		Unit
				-Mxx	-Lxx	
t _{LHLL}	ALE pulse width	Min	2t _{CLCL} -40	2t _{CLCL} -10	2t _{CLCL} -15	ns
t _{AVLL}	Address valid to ALE low	Min	t _{CLCL} -40	t _{CLCL} -15	t _{CLCL} -20	ns
t _{LLAX}	Address hold after ALE low	Min	t _{CLCL} -30	t _{CLCL} -15	t _{CLCL} -20	ns
t _{LLIV}	ALE low to valide instruction in	Max	4t _{CLCL} -100	4t _{CLCL} -30	4t _{CLCL} -35	ns
t _{LLPL}	ALE low to PSEN low	Min	t _{CLCL} -30	t _{CLCL} -10	t _{CLCL} -15	ns
t _{PLPH}	PSEN pulse width	Min	3t _{CLCL} -45	3t _{CLCL} -20	3t _{CLCL} -25	ns
t _{PLIV}	PSEN low to valid instruction in	Max	3t _{CLCL} -105	3t _{CLCL} -40	3t _{CLCL} -45	ns
t _{PXIX}	Input instruction hold after PSEN	Min	0	0	0	ns
t _{PXIZ}	Input instruction float after PSEN	Max	t _{CLCL} -25	t _{CLCL} -7	t _{CLCL} -15	ns
t _{AVIV}	Address to valid instruction in	Max	5t _{CLCL} -105	5t _{CLCL} -40	5t _{CLCL} -45	ns
t _{PLAZ}	PSEN low to address float	Max	10	10	10	ns

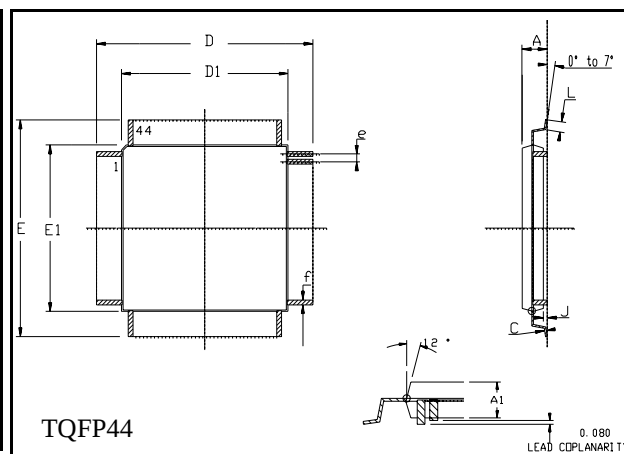
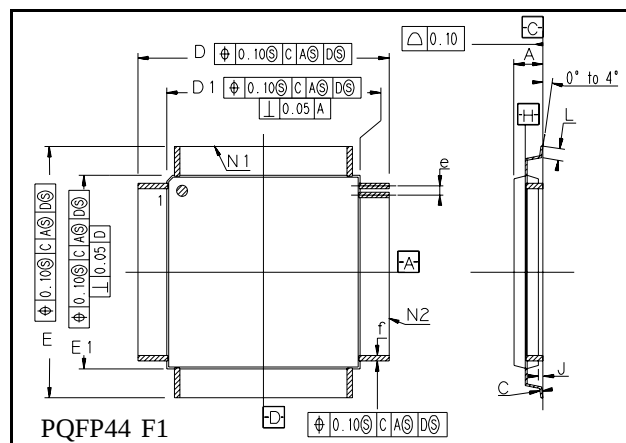
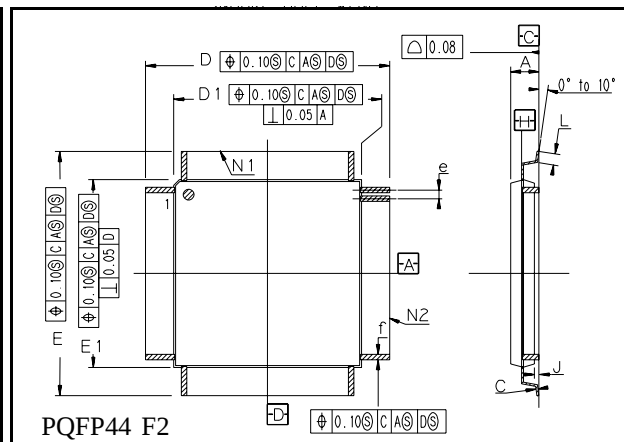
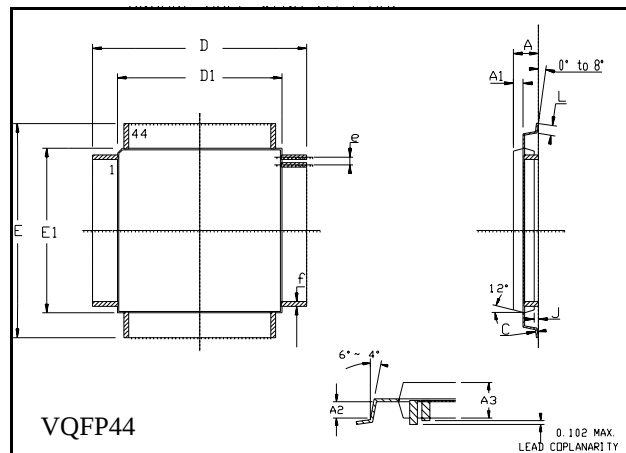
5.2. External Data Memory Characteristics

Symbol	Parameter	Cond.	TSC87C52	TS87C52X2		Unit
				-Mxx	-Lxx	
t _{RLRH}	RD pulse width	Min	6t _{CLCL} -100	6t _{CLCL} -20	6t _{CLCL} -25	ns
t _{WLWH}	WR pulse width	Min	6t _{CLCL} -100	6t _{CLCL} -20	6t _{CLCL} -25	ns
t _{RLDV}	RD Low to valid data in	Max	5t _{CLCL} -165	5t _{CLCL} -25	5t _{CLCL} -30	ns
t _{RHDX}	Data hold after RD	Min	0	0	0	ns
t _{RHDZ}	Data float after RD	Max	2t _{CLCL} -60	2t _{CLCL} -20	2t _{CLCL} -25	ns
t _{LLDV}	ALE low to valid data in	Max	8t _{CLCL} -150	8t _{CLCL} -40	8t _{CLCL} -45	ns
t _{AVDV}	Address to valid data in	Max	9t _{CLCL} -165	9t _{CLCL} -60	9t _{CLCL} -65	ns
t _{LLWL}	ALE low to RD or WR low	Min	3t _{CLCL} -50	3t _{CLCL} +25	3t _{CLCL} +30	ns
t _{LLWL}	ALE low to RD or WR low	Max	3t _{CLCL} +50	3t _{CLCL} +25	3t _{CLCL} +30	ns
t _{AVWL}	Address valid to WR low or RD low	Min	4t _{CLCL} -130	4t _{CLCL} -25	4t _{CLCL} -30	ns
t _{QVWX}	Data valid to WR transition	Min	t _{CLCL} -50	t _{CLCL} -15	t _{CLCL} -20	ns
t _{WHQX}	Data hold after WR	Min	t _{CLCL} -50	t _{CLCL} -10	t _{CLCL} -15	ns
t _{QVWH}	Data valid to to WR High	Min	7t _{CLCL} -150	7t _{CLCL} -15	7t _{CLCL} -20	ns
t _{TRLAZ}	RD low to address float	Min	0	0	0	ns
t _{WHLH}	RD or WR high to ALE high	Min	t _{CLCL} -40	t _{CLCL} +15	t _{CLCL} +20	ns
t _{WHLH}	RD or WR high to ALE high	Max	t _{CLCL} +40	t _{CLCL} +15	t _{CLCL} +20	ns

5.3. Serial Port Timing - Shift register

Symbol	Parameter	Cond.	TSC87C52	TS87C52X2		Unit
				-Mxx	-Lxx	
t _{XLXL}	Serial port clock cycle time	Min	12t _{CLCL}	12t _{CLCL}	12t _{CLCL}	ns
t _{QVXH}	Output data setup to clock rising edge	Min	10t _{CLCL} -133	10t _{CLCL} -50	10t _{CLCL} -50	ns
t _{XHQX}	Output data hold after clock edge	Min	2t _{CLCL} -117	2t _{CLCL} -20	2t _{CLCL} -20	ns
t _{XHDX}	Input data hold after clock rining edge	Min	0	0	0	ns
t _{XHDV}	Clock rising edge to input data valid	Max	10t _{CLCL} -133	10t _{CLCL} -133	10t _{CLCL} -133	ns

6. Packages



		A	C	D	D1	E	E1	e	f	J	L	N1	N2
PQFP44 F2	Min	1.90	0.10	12.10	9.90	12.10	9.90	0.80	0.25	0.00	0.35	11	11
	Max	2.40	0.20	12.50	10.10	12.50	10.10		0.45	0.20	0.65		
PQFP44 F1	Min	2.00	0.10	13.65	9.90	13.65	9.90	0.80	0.20	0.00	0.65	11	11
	Max	2.40	0.20	14.15	10.1	14.15	10.10		0.40	0.30	0.95		
VFQFP44	Min	-	0.10	11.90	9.90	11.90	9.90	0.80	0.35	0.05	0.45	11	11
	Max	1.6	0.20	12.10	10.10	12.10	10.10			-	0.75		
TQFP44	Min	-	0.09	12.00	10.00	12.00	10.00	0.80	0.30	0.05	0.45	11	11
	Max	1.20	0.20						0.45	0.15	0.75		

7. Cross Reference

Old Atmel W&M part	New Atmel W&M part	Old Atmel W&M part	New Atmel W&M part
TSC87C52-16CA	TS87C52X2-MCA	TSC87C52-20CA	TS87C52X2-MCA
TSC87C52-16CB	TS87C52X2-MCB	TSC87C52-20CB	TS87C52X2-MCB
TSC87C52-16CC	TS87C52X2-MCC	TSC87C52-20CC	TS87C52X2-MCC
TSC87C52-16CD	TS87C52X2-MCE	TSC87C52-20CD	TS87C52X2-MCE
TSC87C52-16CE	TS87C52X2-MCE	TSC87C52-20CE	TS87C52X2-MCE
TSC87C52-16CF	TS87C52X2-MCE	TSC87C52-20CD	TS87C52X2-MCE
TSC87C52-16IA	TS87C52X2-MIA	TSC87C52-20IA	TS87C52X2-MIA
TSC87C52-16IB	TS87C52X2-MIB	TSC87C52-20IB	TS87C52X2-MIB
TSC87C52-16IC	TS87C52X2-MIC	TSC87C52-20IC	TS87C52X2-MIC
TSC87C52-16ID	TS87C52X2-MIE	TSC87C52-20ID	TS87C52X2-MIE
TSC87C52-16IE	TS87C52X2-MIE	TSC87C52-20IE	TS87C52X2-MIE
TSC87C52-16IF	TS87C52X2-MIE	TSC87C52-20ID	TS87C52X2-MIE
TSC87C52-L16CA	TS87C52X2-LCA	TSC87C52-25CA	TS87C52X2-MCA
TSC87C52-L16CB	TS87C52X2-LCB	TSC87C52-25CB	TS87C52X2-MCB
TSC87C52-L16CC	TS87C52X2-LCC	TSC87C52-25CC	TS87C52X2-MCC
TSC87C52-L16CD	TS87C52X2-LCE	TSC87C52-25CD	TS87C52X2-MCE
TSC87C52-L16CE	TS87C52X2-LCE	TSC87C52-25CE	TS87C52X2-MCE
TSC87C52-L16CF	TS87C52X2-LCE	TSC87C52-25CD	TS87C52X2-MCE
TSC87C52-L16CJ	TS87C52X2-LCJ	TSC87C52-25CJ	TS87C52X2-MCJ
TSC87C52-L16CK	TS87C52X2-LCK	TSC87C52-25CK	TS87C52X2-MCK
TSC87C52-L16CH	TS87C52X2-LCJ	TSC87C52-25CH	TS87C52X2-MCJ
TSC87C52-L16CI	TS87C52X2-LCK	TSC87C52-25CI	TS87C52X2-MCK
TSC87C52-L16IA	TS87C52X2-LIA	TSC87C52-25IA	TS87C52X2-MIA
TSC87C52-L16IB	TS87C52X2-LIB	TSC87C52-25IB	TS87C52X2-MIB
TSC87C52-L16IC	TS87C52X2-LIC	TSC87C52-25IC	TS87C52X2-MIC
TSC87C52-L16ID	TS87C52X2-LIE	TSC87C52-25ID	TS87C52X2-MIE
TSC87C52-L16IE	TS87C52X2-LIE	TSC87C52-25IE	TS87C52X2-MIE
TSC87C52-L16IF	TS87C52X2-LIE	TSC87C52-25ID	TS87C52X2-MIE
TSC87C52-12CA	TS87C52X2-MCA	TSC87C52-33CA	TS87C52X2-MCA
TSC87C52-12CB	TS87C52X2-MCB	TSC87C52-33CB	TS87C52X2-MCB
TSC87C52-12CC	TS87C52X2-MCC	TSC87C52-33CC	TS87C52X2-MCC
TSC87C52-12CD	TS87C52X2-MCE	TSC87C52-33CD	TS87C52X2-MCE
TSC87C52-12CE	TS87C52X2-MCE	TSC87C52-33CE	TS87C52X2-MCE
TSC87C52-12CD	TS87C52X2-MCE	TSC87C52-33CD	TS87C52X2-MCE
TSC87C52-12IA	TS87C52X2-MIA	TSC87C52-33IA	TS87C52X2-MIA
TSC87C52-12IB	TS87C52X2-MIB	TSC87C52-33IB	TS87C52X2-MIB
TSC87C52-12IC	TS87C52X2-MIC	TSC87C52-33IC	TS87C52X2-MIC
TSC87C52-12ID	TS87C52X2-MIE	TSC87C52-33ID	TS87C52X2-MIE
TSC87C52-12IE	TS87C52X2-MIE	TSC87C52-33IE	TS87C52X2-MIE
TSC87C52-12IF	TS87C52X2-MIE	TSC87C52-33ID	TS87C52X2-MIE

8. Bibliography

Atmel W&M TSC87C52 datasheet (Rev C, 10 Sept 1997).

Atmel W&M TS80C32X2, TS80C52X2 and TS87C52X2 datasheet Rev. B (Aug. 1999).